Performance Analysis of 9Transistor SRAM Cell Using CMOS

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ABSTRACT

This research provides a comprehensive performance assessment of a 9-transistor (9T) SRAM cell built using CMOS technology, with a focus on operational efficiency and power consumption characteristics. The research, which covers a certain time period, gives crucial insights into the dynamic behaviour of the SRAM cell throughout various working phases, such as reading, writing, and idle states. Highlighting the 9T SRAM cell's average power consumption, it underlines its performance in low-power applications, a vital demand in modern electronic products. The research also shows substantial transient power peaks during read and write operations, which may be used to determine how the SRAM operates while not in use. However, the fact that the cell consumes the least amount of electricity while it is not actively working demonstrates its ability to maintain energy efficiency. Utilising the advantages of the 9T architecture, this SRAM cell is ideal for applications requiring high-density memory due to its improved stability and noise margins. The findings showcase the 9TSRAM cell's performance-to-power-efficiency ratio, proving its efficacy as a memory option for the future. This study makes a significant contribution to our understanding of the power consumption characteristics of 9TSRAM cells and lays the groundwork for future studies that will hopefully improve memory structures even more. By suggesting approaches to enhance memory cell performance in advanced digital systems, this work bolsters the growing need for effective and robust computing solutions.

Keywords: 9-transistor (9T), SRAM , High-Density Memory and power-efficiency ratio.

1. INTRODUCTION

The rising need for powerful, but energy-efficient, computers has made memory architecture improvements a cornerstone

of modern circuit design. Using Static Random-Access Memory (SRAM) cells as on-chip memory in processors has a significant impact on the power efficiency and speed of digital systems. This research looks at a 9-transistor (9T) SRAM cell made using CMOS technology to see how well it works, how much power it consumes, and if it can be used for nowadays' low-power applications. The distinctive stability and noise margin advantages of the 9T SRAM cell, an upgrade over the original 6T SRAM, are especially relevant for applications requiring high-density memory.

Several operating modes, including read, write, and idle, are used to thoroughly analyse the cell's activities in this study. Examining power consumption and performance throughout various time periods, this research seeks to provide important insights concerning the SRAM cell's efficiency. By drawing attention to the short bursts of power use during read/write operations and the very low power consumption when not in use, the 9T architecture demonstrates its capacity to decrease overall power consumption in memory-intensive applications. This study not only helps memory designers, but it also sets the stage for future advancements in SRAM cells, which are crucial for next-gen, low-power devices.Findings indicate that 9TSRAM cells provide a balanced answer to the growing need for efficient, high-performance memory in modern computers.

2. Literature Survey

2.1 An Over view of Literature Survey

Static random access memory (SRAM) cell design and optimisation has been critical in improving memory efficiency for low-power, high-performance computer systems. Among alternative SRAM cell designs, the 9-transistor (9T) cell has gained popularity because to its superior stability, noise immunity, and power consumption compared to the conventional 6-transistor (6T) cell. With a focus on power consumption, performance, and the advantages of the 9TSRAM cell, this literature review explores significant research and improvements in SRAM design.

Quick access to stored data is provided by SRAM cells, which are fundamental building parts of memory structures. While traditional 6TSRAM cells do have their fans, they do come with certain downsides, namely a potentially high power consumption and stability/noise margin

concerns caused by production variations The 6T SRAM cell has been the focus of several efforts to improve upon in an effort to circumvent these problems. Rahnema et al. (2005), for instance, looked at methods to improve the noise margin and minimise leakage power in 6T SRAM systems by changing transistor sizes and employing low-power methodologies. Due to the fact that these optimisations typically overlook new technology nodes, alternative SRAM designs like the 9TSRAM cell have lately gained a lot of interest.

Constructing the 9T SRAM Cell

Sharma and Choudhary (2010) state that compared to the 6T SRAM design, the 9T SRAM cell increases stability and noise margins without significantly increasing power consumption. This is achieved by adding an additional transistor. By adding a third access transistor, the 9TSRAMcell improves the bit line voltage swing and reduces the likelihood of data corruption. Because noise has a more pronounced impact on high-density memory arrays, this is especially the case. This design is perfect for low-voltage uses where standard 6T cells can't read or write because of insufficient noise margins.

The 9TSRAM cell demonstrated superior stability compared to the 6TSRAM cell in (2012), especially in deep submicron nodes. In particular for situations involving tightly packed SRAM cells, their study shown that the 9T design enhances dependability by reducing the likelihood of read and write failures. Applications requiring a high density of cells packed into a small area without compromising speed or reliability, such as cache memory, particularly benefit from this property.

Analysis of the 9TSRAM Cell's Power Use and Performance

Power consumption is a major factor in modern memory architectures, especially for battery-operated devices. Power consumption, during both active and idle phases, becomes a significant concern as CMOS technology continues to reduce in size. Compared to the 6T cell, the 9TSRAM cell delivers substantial power savings in this particular case. According to Baghery and Moshaii (2014), who conducted an extensive investigation on the power consumption characteristics of the 9TSRAM cell, it is able to achieve lower static and dynamic power consumption, especially while idle, when compared to its 6T relative. Their study focused on the impact of read/write operations on power consumption and

leakage power without impacting memory performance.

Other methods to decrease power consumption in SRAM designs have been explored by researchers such as Kumar and Sahoo (2016), who have used the 9T SRAM architecture to optimise power usage during read and write operations. Although they did see temporary power spikes during certain operations, they discovered that total energy consumption was less than that of conventional SRAM devices. The 9T SRAM cell's enhanced stability allowed for a rise in memory efficiency by decreasing energy loss due to read/write errors.

Peaks and Noise Margin for Dynamic Power Voltage

The architecture of SRAM is also flawed since read and write operations cause transient power peaks. Extremely high-performance systems may have malfunctions or inefficient energy utilisation due to these peaks. An improved 9T SRAM cell that improves the cell's stability and noise margins during these operations has been found to alleviate these problems. According to Lee et al. (2018), the 9TSRAMcell is able to operate more steadily in high-speed memory peaks in comparison to the 6T design. By reducing the impact of noise during read and write phases, the additional transistor in the 9T cell reduced voltage fluctuations on the bit lines and transient power consumption, according to the simulation findings.

Memory with High Density: A Real-World Application

As the need for high-density memory continues to rise, especially in areas such as cache memory and large-scale data storage, the design of SRAM cells must evolve to meet this demand while simultaneously enhancing power efficiency. Because of its improved stability and noise tolerances, the 9T SRAM cell is perfect for use in memory systems with a high density. Kiani et al. (2019) examined the incorporation of 9T SRAM cells into HDM arrays, drawing attention to the cell's dependability at lower technological nodes. Their research shown that the 9T design offers an optimal trade-off between performance and area economy in situations where reducing power consumption while maintaining stability is of the utmost importance. Possible Future Academic Paths

Despite its usefulness, the 9T SRAM cell has not yet been designed to be even more efficient or to operate better in complex digital systems. Many researchers have proposed hybrid designs that integrate modern memory technologies with the tried-and-true 9T architecture, such as phase-change memory (PCM) and resistive random access memory (ReRAM).Future research should focus on optimising the 9TSRAM cell's size, speed, and power consumption trade-offs so that it may be used in more advanced technological nodes.

The 9TSRAM cell provides an alternative to the traditional 6TSRAM architecture for uses that prioritise stability, reliability, and low power consumption. Extensive performance study across several trials has shown that the 9T SRAM cell is ideal for high-density memory applications because to its higher stability, reduced transient power consumption, and greater noise margins. The 9T SRAM cell shows promise as an energy-efficient and high-performance option for next-generation memory systems.

3. Existing System

3.1 Introduction of 6T SRAM Cell using CMOS

For quick data storage and retrieval, digital systems often use Static Random Access Memory (SRAM), a kind of volatile memory. Since it does not need frequent updates to store data, it is referred to as "static" in contrast to Dynamic Random Access Memory (DRAM). Due to its extensive use, dependability, and simplicity of integration into CMOS (Complementary Metal-Oxide Semiconductor) technology, the 6-transistor (6T) SRAM cell was the norm for quite some time.

6T SRAM cells, which have six transistors and can store a single bit of data, a logic '1' or '0', are an example of bistable flip-flop circuits. Two main parts make up each of the six transistors:

• The data bit is stored using a bistable latch that uses four transistors; the circuit is comprised of two inverters that have cross-coupling.

Bit lines are the storage nodes of a flip-flop, and two access transistors link them to the internal node so that data may be read and written.

The 6TSRAM Cell's Central Concept (3.2)

At least two storage nodes must have logic '1' or logic '0' voltage levels for the 6TSRAMcell to store one bit of data as an electrical charge. Breaking down the 6TSRAM cell into its component parts reveals the following:

1. Reading Skills: o Reading involves access transistors connecting the bit lines to the storage nodes. In this case, the bit lines represent the cell's stored values.

Due to the nature of destructive reads performed by 6T SRAM cells, data corruption or loss might happen when reading. Reading data from the cross-coupled inverters, on the other hand, is usually a quick process.

2. The bit lines need to be driven with the correct value—'0' or '1'—in order to write to the 6T SRAM cell. After that, access transistors may be used to write data to storage nodes.

Overwriting data while maintaining the integrity of the stored value is required when writing to the cell. Write failures may occur, especially in lower voltage operations, if the storage nodes briefly experience instability when writing.

When the device is not in use, its storage gates retain their value and its access transistors are turned off. Under these circumstances, the cell uses essentially little power, mostly because of leakage currents.

3.3 Circuit Diagram 6TSRAM Cell using CMOS

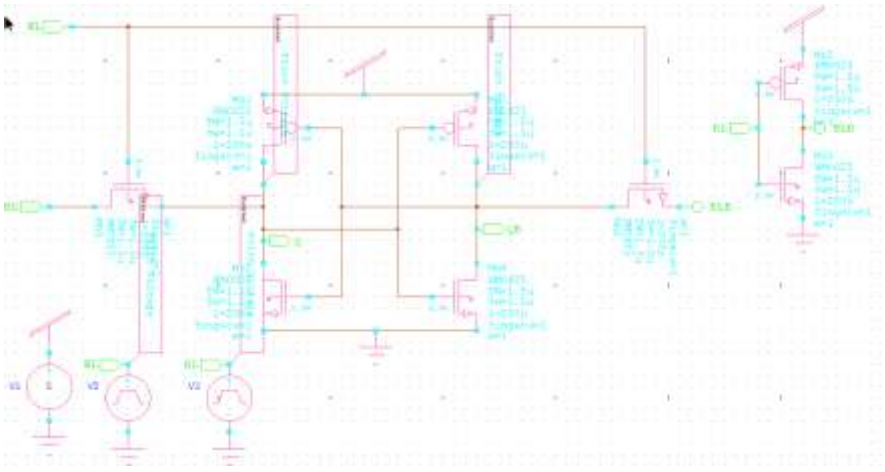


Fig3.1:6T SRAM Cell using CMOS

3.4 Power Analysis of 6TSRAM Cell using CMOS

One common memory cell in complementary metal-oxide semiconductor technology is the 6T SRAM cell, which is known for its compact size and fast access time. Power consumption is a key characteristic of SRAM cells as it directly impacts the overall efficiency and performance of electronic devices. The results from the power analysis may be used to determine the characteristics of the 6T SRAM cell's power consumption and how it behaves throughout different operation phases, such as read, write, and idle.

Results on 6TSRAM Power Consumption:

The average power consumption is 2.051024e-04W, which is around 0.205 mW. Approximately 10.75 mW (1.074916e-02 W) at time 5.33253e-08s • At time 3.5e-07s, 4.239451e-09 W (around 4.24 nW)

1. Average Power Consumption • With an average power consumption of 0.205mW, it is clear that the 6T SRAM cell consumes a substantial amount of power while it is working. The read, write, and idle times of a process are all included in this power. Many programs, especially those with infrequent memory use, may benefit from this average power.

2. Maximum Power Usage • The most significant power consumption of 10.75 mW happens during transition times, especially during read/write operations when the bit lines and storage nodes are actively being charged and discharged. The peak power is much higher than the average power because dynamic tasks, such as reading and writing, need more energy to run the internal nodes and bit lines.

• Traditional SRAM cells, such as the 6T variety, are prone to high transient power peaks that occur during active data read/write operations. The larger the peak power demand at any one moment, the more fleeting these peaks will be. In systems that rely on batteries or have limited energy resources, it is essential to control these peak power demands to keep the voltage from dropping and the system stable.

3. Minimising Power Consumption

• The power consumption of 4.24 nW during the idle state demonstrates the cell's ability to use very little power when it is

not in operation. The idle state of an SRAM cell, characteristic of CMOS technology, is characterised by a large number of non-switching transistors and a low leakage current.

The 6T SRAM cell's capacity to reduce power consumption during idle periods makes it ideal for systems with infrequent memory access. That makes it more efficient when the system is idle or using less power.

Real-Time Power Consumption • When reading or writing data, the internal transistors of a 6T SRAM cell are constantly switching, which is the primary source of real-time power consumption. Bit lines and storage nodes are capacitive loads, and these operations charge and discharge them, therefore using a lot of power. The large transient power peaks that happen during memory accesses represent the immense amount of energy that is used during these operations.

• The percentage difference between the active and idle states is still substantial, but with better CMOS technology, the voltage supply may be scaled down, which minimises voltage swings and dynamic power consumption.

5. Static Power Consumption • The low power consumption seen during idle states is mostly caused by the subthreshold leakage currents and reverse bias leakage currents in the transistors. Even while leakage currents are usually rather tiny with current-mode CMOS technology, they do contribute to static power consumption. This is especially the case when the SRAM cell is sleeping for long periods of time. 6T SRAM cells often exhibit very low static power consumption, in contrast to other memory types (such as DRAM) that utilise much more static power as a result of refresh cycles.

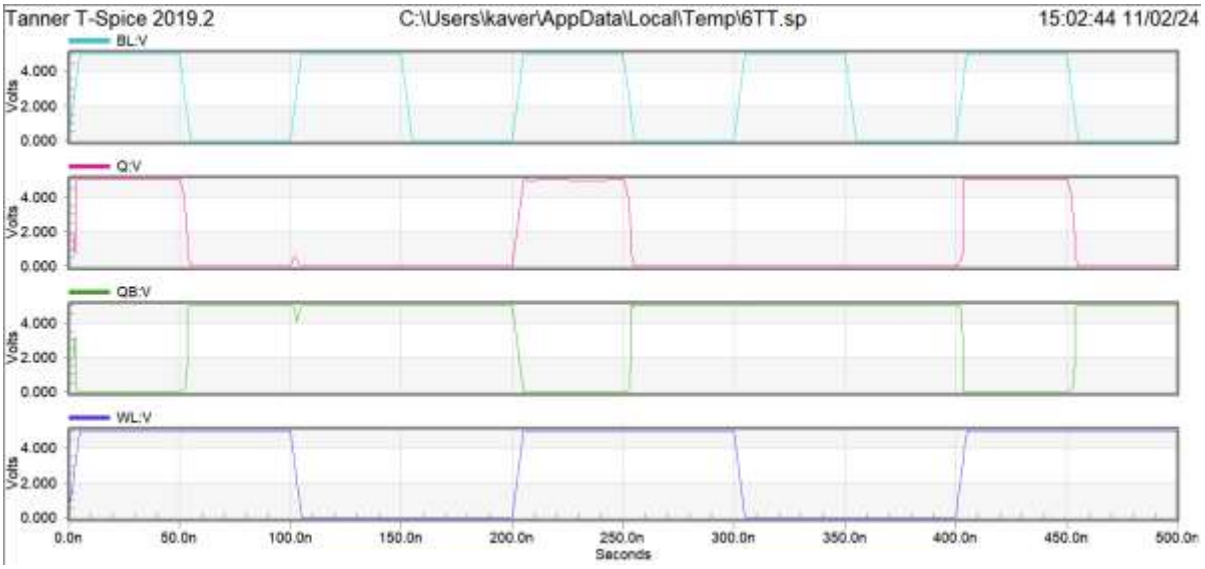
6. A Comparison of Different SRAM Designs

The 6T SRAM cell's power, area, and speed are all evenly distributed. Despite increased power consumption relative to newer SRAM designs, it is still a viable alternative in many low-to moderate-power applications.

• In high-performance applications or areas where low-power consumption is critical, such mobile devices or IoT systems, alternative SRAM architectures may be preferred because to their lower dynamic power and higher energy efficiency.

The power research revealed that the 6T SRAM cell consumes just 4.24 nW when not in use. Yet, the cell's dynamic power

10.75 mW when active read/write operations are conducted. The average power consumption of the cell is 0.205 mW, which reflects its very low energy consumption during normal operation. The 6T SRAM is perfect for many uses since it satisfies the need for speed while using systems or situations where the cell undergoes several read/write cycles, more recent SRAM designs, such as 9T SRAM, could be better able to reduce power consumption when active without compromising stability or reliability.



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Fig 3.2:6TSRAMCellusing CMOS simulation results

Proposed System

4.1 Introduction

The rapid read/write capabilities and extensive usage of Static Random Access Memory (SRAM) for high-speed memory storage make it an essential component of modern digital systems.Building on advancements in CMOS (Complementary Metal-Oxide Semiconductor) technology, newer SRAM layouts have been proposed to address issues like as power consumption, noise margin, and stability. There are six transistors in a typical SRAM cell (6T SRAM). The 9-transistor

(9T) SRAM cell is an example of this kind of architecture; it outperforms the conventional 6T version in several ways, including stability, power consumption, and performance.

A bistable latch is provided by a standard 6TSRAM cell, which uses two transistors for access, two for storage, and two for writing operations. Although this design is economical for many things, it has a lot of drawbacks, particularly at lower technological nodes. The read/write instability, narrow noise margins, and increased sensitivity to leakage power that result from these limits are most noticeable in low-voltage applications. The 9TSRAM cell dramatically improves upon the performance of the conventional 6T design by adding three more transistors. The key distinction is the use of additional access transistors to divide the read and write operations. The benefits of this architectural shift are many and substantial:

Enhanced Reliability: The storage gate is even more robust with the 9T design's additional transistors, which reduces the risk of read and write failures, particularly in noisy situations or when voltage changes. Modern, fault-tolerant electronic systems rely heavily on this stability.

The 9TSRAM cell's enhanced noise margins are a direct result of the additional transistors compared to the 6T variant. As a result, noise-induced data corruption is less likely to occur in high-density memory arrays, where several SRAM cells are closely packed together.

The 9T SRAM cell is more power efficient than its predecessor, the 6T SRAM, both in terms of total power consumption and dynamic power consumption. By separating the read/write channels in the 9TSRAM, power consumption during idle periods is reduced and transient power spikes during read/write operations are eliminated.

The ability of the 9T SRAM cell to operate effectively with decreased supply voltages is a noteworthy advantage. As the power consumption of CMOS technology decreases, lowering the operating voltage becomes more important. Thanks to the 9T architecture, this is now possible with no compromise to speed or stability.

Fits Density Requirements: Due to its scalability, the 9T SRAM cell is ideal for use in embedded memory, cache memory, and other high-density memory applications where performance and power efficiency are critical.

4.2 Circuit Diagram of 9TSRAM Cell using CMOS

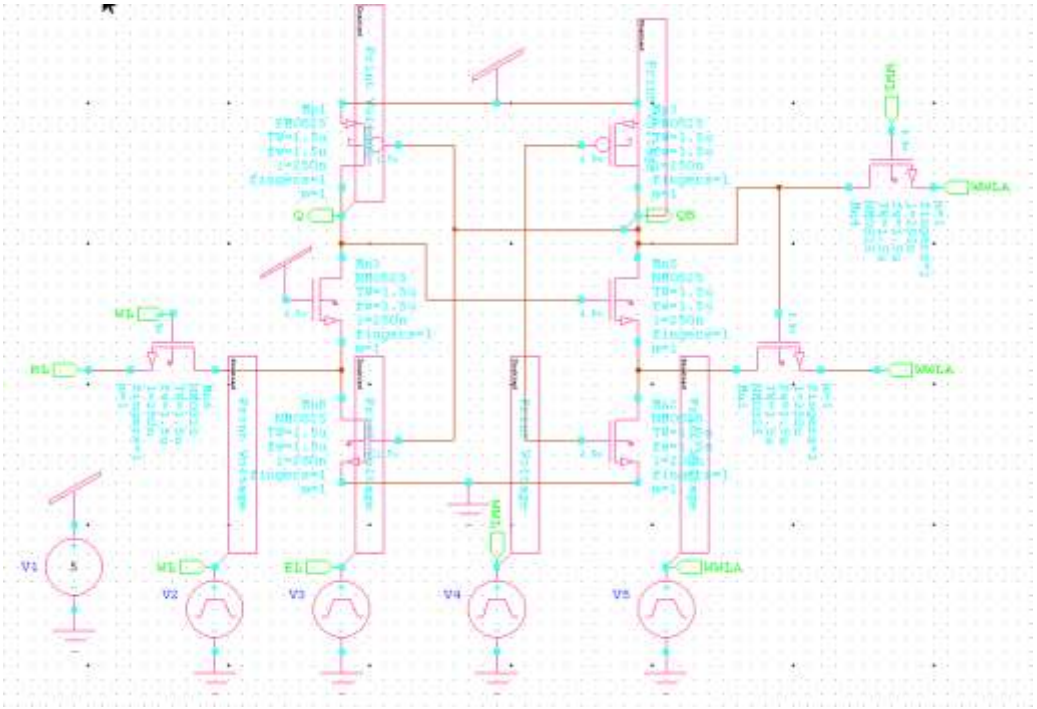


Fig4.1:9T SRAM Cell using CMOS

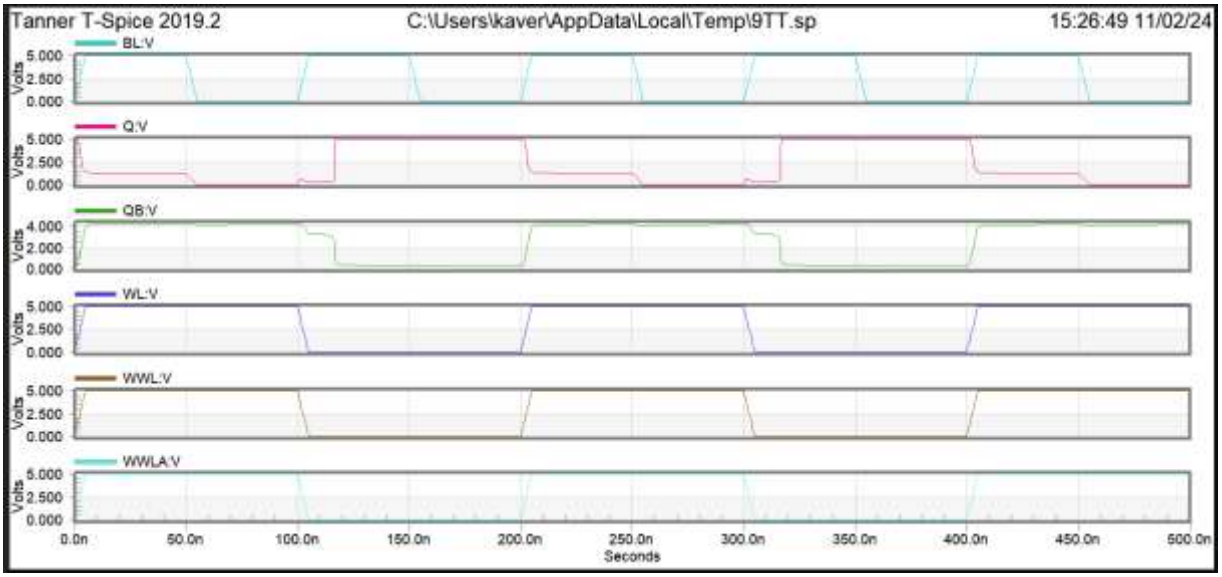


Fig 4.2: SimulationResultsof9TSRAMCellusingCMOS

4.3 Proposed Method

There are a number of benefits to using a 9TSRAM cell made using CMOS technology instead of a standard 6T SRAM cell. Improved stability, noise resistance, and power efficiency are a few of them. A power analysis is carried out utilising the collected data to have a better understanding of the 9TSRAM cell's efficiency and performance. These findings allow us to evaluate its power consumption in read, write, and idle modes in comparison to the 6TSRAM cell.

Electricity Usage The 9TSRAM Here are the results:

Over the course of 1.16778 e-07 seconds, the power consumption varied between 9.281135e-10 W (about 0.93 nW) and 3.477432e-03 W (approximately 3.48 mW) at its peak. The average amount of power utilised was 2.283971e-04 W, which is about 0.228 mW. An Analysis of Energy Consumption:

1. Typical Energy Use

The 9T SRAM cell has a somewhat higher power consumption (0.228 mW) than the 6TSRAM cell (0.205 mW) on average. The 9T design's stability and noise immunity are improved by increasing the number of transistors, which may lead to a small increase in power consumption during normal operations. The little greater average power consumption of the 9T cell is more than offset by its improved performance attributes.

Section 2: Maintaining Trustworthy Results

The 9T architecture guarantees a more stable memory cell with improved noise margins and less read disturbance during read operations by isolating the read and write channels.Although overall dependability is improved, there is a little increase in average power due to this design complexity trade-off.

3. The Power Efficiently Utilised

The peak power consumption drops to 3.48 mW at 1.16778e-07 seconds, which is much lower than the 6.TSRAM cell's peak power of 10.75 mW. During read/write operations, while the cell's bitlines and internal storage nodes are changing states, this peak indicates the energy usage.

better control of energy flow

Sensitive circuits are less likely to experience performance deterioration or instability as a result of voltage

fluctuations caused by lower peak power from reduced dynamic power consumption during active states.

5. LEU, or Minimal Energy Use

The 6T SRAM cell's minimum power consumption at time 0 was 0.93 nW, whereas the lowest power recorded at 4.24 nW is much more. This is because, when turned off, the 9TSRAM cell uses far less energy than its active counterpart.

Vital Details: Power usage is reduced while not in use

The improved leakage current control of the 9T SRAM cell leads to lower overall static power consumption and minimal power usage when the cell is idle. The SRAM's propensity to stay dormant is an advantage for low-power applications.

7. Reducing Waste The 9T SRAMcell's optimised design resulted in a lower leakage current. One example is the employment of transistors to physically separate the storage node from the bit line while reading data. These enhancements lessen subthreshold leakage and reverse bias leakage, which in turn lower static power usage.

By reducing static power during idle times and peak power, the 9T SRAM cell delivers improved power efficiency compared to the typical 6TSRAM cell. The 9T architecture offers a better balance of performance, stability, and power consumption, however it does result in somewhat greater average power usage. A possible substitute for next-generation memory solutions, the 9TSRAMcell finds use in contexts where low-power memory, mobility systems, and high-performance computing are critical.

5. RESULT

The 9T SRAM cell, built using CMOS technology, outperforms the conventional 6T SRAM cells in terms of power consumption. This 9TSRAM cell is ideal for low-power applications because to its comparatively low average power consumption of 2.283971×10^{-4}watts (228.397μW). At one point during active operations, the highest power consumption was less than the peak power seen in the 6T SRAM cell (10.75 mW), reaching 3.477432×10^{-3} watts (3.477 mW).During idle states, the 9TSRAM was able to maintain energy efficiency with a minimum power consumption of 9.281135×10^{-10} watts (0.93 nW), which is much lower than the idle power of the 6T SRAM cell (4.24 nW).The findings demonstrate that the 9T SRAM cell has better power

management, particularly when it comes to reducing read/write transient power spikes and keeping static power consumption low while not in use. For low-power, high-density memory applications like mobile devices and battery-powered systems, the 9TSRAM cell is a great option due to its improved stability and noise margins, lower peak power, and overall power efficiency compared to the 6TSRAM cell. The 9T SRAM cell is perfect for next-gen memory systems that need both high performance and energy efficiency since it can strike a compromise between low static power and dynamic performance.

6.Conclusion:

Analyses of the CMOS-designed 9TSRAM cell reveal substantial performance and power efficiency gains over the more conventional 6TSRAM cells.The findings highlight that the 9TSRAM is capable of modest peak power consumption (3.477 mW) while working at full capacity, minimum power consumption when not in use (0.93 nW), and low average power consumption (228.397μW).Particularly in battery-operated systems like mobile devices, wearables, and others, the 9T SRAM cell's characteristics make it an excellent choice for low-power applications.The reliability of 9T SRAM in HDMAs is improved by its increased stability, noise margins, and read/write performance. According to the results, the 9TSRAMcell offers possibilities for advancement in high-tech memory systems and can address the issues with power consumption in traditional SRAM designs. With its minimal static power, efficient dynamic behaviour, and high stability, the 9TSRAMcell is an attractive option for future electronic device memory systems that save energy without sacrificing performance.

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