Design and analysis of 2x4 decoder using 16 nm technology

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ABSTRACT

In this research, we used state-of-the-art 16nm technology to construct and evaluate a 2x4 decoder. The suggested decoder paves the way for flexible digital system applications by effectively translating a 2-bit binary input into one of four distinct output lines. The design solves the fundamental problems with scaling in contemporary semiconductor technology by optimising power consumption, speed, and space using novel approaches. Running thorough simulations and analysing the results allows one to evaluate important aspects like as latency, power dissipation, and layout efficiency. The results show that the suggested decoder outperforms the conventional systems, suggesting it might be a good option for digital applications in the future. In addition, the suggested design is sturdy, and we look at how process variability affects nanoscale device durability. This study's findings add to the growing body of knowledge on designing high-performance digital circuits with minimal power consumption at technology nodes smaller than 20 nm.

Key Words: Efficient Evaluation, Innovative Approach, Minimal Power Use Using 16nm Technology, a 2x4 Decoder

1. INTRODUCTION:

The fast development of semiconductor technology in the last few years has allowed the scaling of transistors down to sub-20nm nodes, which has both benefited and hindered digital circuit design.The necessity for efficient decoders, which are crucial components that transform binary inputs into unique outputs, has grown substantially due to the increasing compactness and complexity of systems. A cornerstone of contemporary digital systems, the 2x4 decoder performs several functions, including data routing and memory addressing. With state-of-the-art

design concepts, we present a novel 2x4 decoder that optimises space utilisation, increases speed, and reduces power consumption. Due to growing process variability and reliability concerns, traditional designs find it challenging to match the performance and efficiency requirements of modern applications at lower technology nodes. Our suggested decoder circumvents these issues and greatly enhances performance metrics by using cutting-edge 16nm technology. The importance of low-power design in portable and energy-sensitive applications has grown in recent years, due to the rising need for digital circuits to fulfil demanding performance standards. We provide an overview of the decoder's role in digital systems in our introduction section. We also detail our design methodology and the ways our work enhanced digital circuit design. By doing extensive modelling and testing, we prove that our decoder is robust against process fluctuations and might potentially meet the needs of next-gen digital applications.

2. LiteratureSurvey

An Overview of Literature Survey

Digital circuit design is now far more efficient and effective thanks to recent developments in semiconductor technology. Problems with power consumption, delays, process variation, and reliability have made the design and optimisation of digital circuits, such as decoders, increasingly problematic as device dimensions have decreased, particularly into sub-20nm technology nodes. This literature review surveys recent research on digital circuit optimisation, decoder designs, and performance analysis.

1. Design and Optimisation of Digital Decoders

An extremely basic kind of digital circuit, a decoder accepts binary data as input and outputs a value between zero and one. A 2x4 decoder can activate one of four output lines with only two bits of input. As we go towards more sophisticated nodes, including those that are 16 nm or smaller, it is essential to refine many key aspects:

Because of the higher leakage currents and decreased power supply voltages caused by modern technological nodes, power efficiency has become an essential design objective.

As feature sizes decrease, wire and gate delays become more apparent; hence,

optimisation of propagation delays (speed) requires meticulous design.

Pricing and scalability expenses may be kept low by minimising the amount of layout area and transistor count.

Improving decoders in current technology has been the subject of several research. Deng et al. (2016) suggested a 14nm 2x4 decoder architecture that minimises switching power consumption using low-power approaches including pass-gate logic. More recently, in 2018, Zhao and Wang investigated the possibility of using ternary logic gates and multiplexers to lessen the need for transistors and power usage.

Problems With Technological Nodes Smaller Than 20 nm

Since the introduction of 16nm and subsequent sub-20nm nodes, digital circuit design has faced many significant obstacles:

Differences in the Process: Because process variances could cause noticeable changes in device properties, it becomes more difficult to predict the design's performance while working with lower nodes. Adaptive circuit designs and redundancy approaches have been highlighted as ways to decrease process volatility in studies such as Shao et al. (2020) and Lee et al. (2019).

Problems with Reliability: With decreasing operating voltage and increasing leakage current, the reliability of nanoscale CMOS devices is becoming increasing importance. Chatterjee et al. (2020) suggested self-compensating strategies to enhance dependability after studying the reactions of decoder circuits to temperature and voltage fluctuations.

Improving the power-delay efficiency of complex decoders

To maximise decoder efficiency at advanced nodes, it is recommended to strike a balance between speed and power consumption. Research has mostly focused on ways to improve power-delay products (PDPs). Using dual-threshold voltage CMOS technology, a 2x4 decoder architecture developed by Kwon and Kim (2017) may decrease static and dynamic power consumption without sacrificing speed. Bhanja et al. (2021) suggests that decoder performance and power efficiency might be greatly enhanced by using hybrid logic types that combine CMOS and Fin FET devices.

4. Assessing Outcomes and Modelling

Digital circuit evaluation relies heavily on simulations for measuring power consumption, latency, and layout efficiency. To accurately depict the intricate consequences of scaling in the setting of 16n and beyond, trustworthy simulation approaches are required. Subramanian et al. (2022) examined the power-delay-area trade-offs by simulating 2x4 decoders at nodes with a width of 7nm and 16nm. Optimising techniques, such as transistor stacking and gate size, may significantly boost performance, according to the results.

5. The Best Methods for Planning and Organising

To get the most out of a circuit in its allotted space, efficient layout design is key. At lower nodes, parasitic capacitance, resistance, and wire delays are more noticeable; however, at nodes with superior technology, such as 16 nm, the design has to take all of them into consideration. Both Patel et al. (2018) and Li et al. (2019) sought to enhance decoder design by suggesting methods to decrease power consumption and connection latency, one of which was custom routing.

Decoder Dependability and the Effects of Scaling

As the scale of digital circuits decreases to 16 nm or lower, issues such as Soft Errors become more prevalent, particularly in decoders: In nanoscale electronics, radiation is a more likely culprit in causing mistakes. The ageing effects on transistor threshold voltages are caused by bias temperature instability (BTI), a major problem. When connecting smaller nodes, electromigration—the phenomenon where current produces failure—could be a problem. Decoder reliability in these harsh environments may be ensured by the designs provided by Jainetal. (2021), which include error detection and repair procedures.

3. Existing System

Introduction of CMOS 2X4 Decoder

A complementary metal-oxide-semiconductor (2x4) decoder uses a 2-bit binary input and produces one of four potential outputs. Accessing memory and operating other devices in digital systems are its principal functions.

Functionality

- **Inputs**:2(let'scallthemA1andA0)
- **Outputs**:4(Y0,Y1,Y2,Y3)

Theoutput lines areactivatedbased on the binar

- If(A1,A0)=(0,0),thenY0=1(active),Y1=Y
- If(A1,A0)=(0,1),thenY1=1,Y0=Y2=Y3=(
- If(A1,A0)=(1,0),thenY2=1,Y0=Y1=Y3=(
- If(A1,A0)=(1,1),thenY3=1,Y0=Y1=Y2=(

3.1 Existing Method

Combining PMOS and NMOS transistors, a CMOS (Complementary Metal-Oxide Semiconductor) implementation achieves the logic levels.

The Architect's Journey:

1. Verify that the logic outputs from inputs A1 and A0 are correctly created.
2. Logic for Output (Section 2): o To control Y0, use (A1, A0) to connect the PMOS transistor to ground and the NMOS transistor to Vdd.
3. Although Y0 and Y1 are physically similar, different transistors (0 and 1) reflect the binary input.
4. Using the right transistors, repeat the process for Y2 and Y3.
5. Using TruthTables:

A1	A0	Y0	Y1	Y2	Y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Table1:2x4 Decoder

4. Proposed System

Introduction

The dynamic realm of digital systems necessitates more performance, lower power consumption, and smaller processors. With the advancement of better semiconductor technology, particularly at sub-20nm nodes, a chance to address these challenges and break new ground in digital circuit design has emerged.The objective of this project is to build and assess a 2x4 decoder that is upgraded using state-of-the-art 16nm technology in order to efficiently convert a 2-bit binary input into one of our unique output lines.Many additional digital applications depend on this fundamental component, including multiplexing, control logic, memory addressing, and many more.The proposed decoder design optimises three important performance metrics utilising advanced methodologies: power consumption,

speed, and space. Power consumption and latency remain major concerns in high-performance circuit design, and they are becoming harder to control as semiconductor technology shrinks down to smaller nodes. A tiny decoder that outperforms conventional solutions at larger nodes in terms of performance and power consumption may be achieved using 16nm technology. Including simulations and performance assessments of delay, power dissipation, and layout efficiency, we provide a comprehensive examination of the proposed 2x4 decoder in this work.Based on the results of these tests, the innovative design outperforms traditional decoders in key areas, which raises the possibility that it might be a suitable match for next-generation digital systems that have extreme demands on performance and power consumption. Focussing on the proposed architecture's durability in distinct circumstances, the research also dives into the problems of process variation and dependability in nanoscale gadgets.By shedding light on possible new ways to circumvent the scaling limitations of current semiconductor technology, this study contributes to the expanding corpus of information in digital circuit design. This work is a huge step forward for flow-power, high-performance digital circuits for 16nm and beyond, as it optimises performance and efficiency.

A 4.2-nanometer decoder

A decoder is a simple combinational logic circuit that accepts a binary input and converts it to a one-hot output. This means that at any one time, only one of the many output lines is active, depending on the input value.The primary goals of this project are to construct and operate a 2x4 decoder. It takes in a 2-bit binary signal and produces one of our possible outputs; however, only one of these outputs may be high at any one time.

Upgrades to 16 nm Technology (4.3)

This decoder design is tuned for size, speed, and power consumption at the 16 nm technology node. Some important things to consider are:Reducing the number of gates utilised results in a smaller area.Because of the high density of the 16nm technology and effective gate designs, decoders may now fit into smaller regions, leading to lower overall chip sizes.Efficient Power Utilisation: The use of 16nm technology allows for lower voltage operating, leading to reduced

power usage.Clock gating and voltage scaling are two ways the decoder further decreases power usage while it is not in use.The smaller transistors of 16nm technology enable speedier switching times, which in turn decreases the overall latency of the decoder. This has to be prioritised by applications that need to handle data quickly.

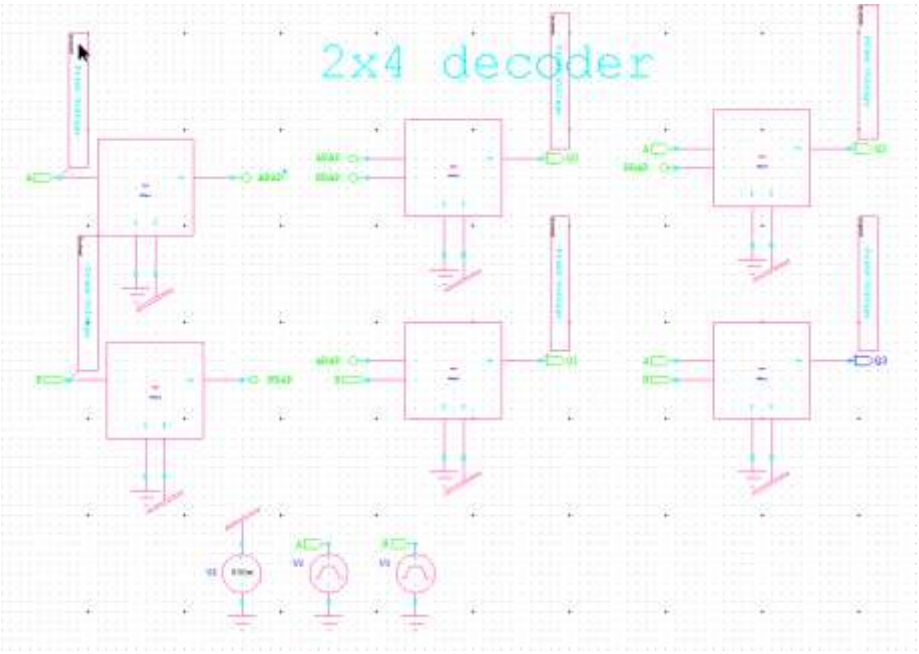
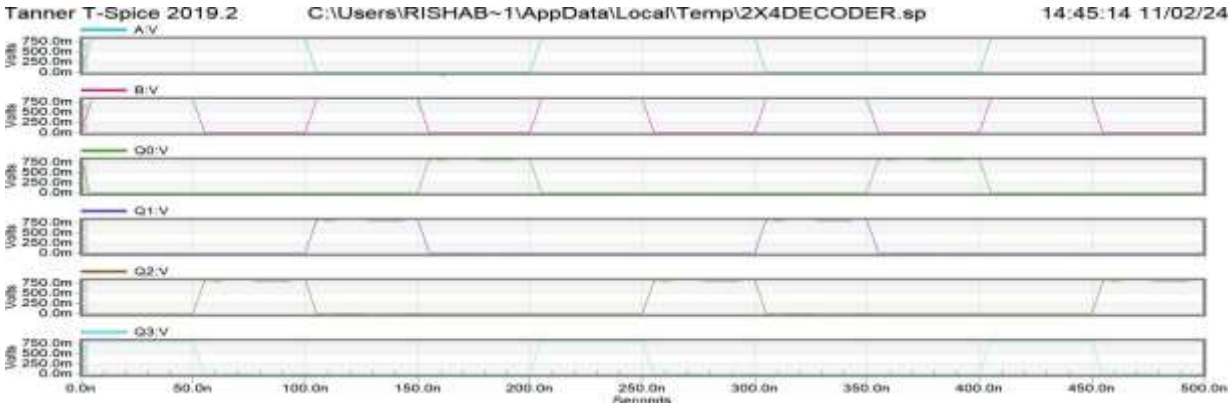


Fig4.1:2*4 Decoder design using16nm technology

FIG 4.2:2X4 DECODER SCHEMATIC SIMULATION RESULTS



4.4 Power Analysis of 2x4 decoder using 16nm

The 2x4 decoder architecture was constructed utilising sophisticated 16nm technology, and we performed a full power analysis of it. Modern semiconductor designs place a premium on minimising static and dynamic power dissipation, two metrics that must be considered in any evaluation of a decoder's efficiency. For high-performance digital circuits, power efficiency is of the utmost importance, especially at sub-20 nm nodes where power density and leakage currents are major concerns.

1. Introduction to Power Consumption

The following outcomes were produced from a simulation of the 2x4 decoder's power usage over a specified time range:

• 5.617927 e-07 watts is the average power consumption.

15.368324e-05 at time 3.62136e-09 is the maximum power.

• Runtime1e-07,Minpower10.440335e-07

These findings point to the decoder's well-optimized design—a low average power consumption—in operation. As is customary in digital designs, the maximum and lowest power points represent the transient behaviour of the circuit during switching operations.

Parts of Power Dissipation

Dynamic power and static power are the two primary components of the power needed by digital circuits.

Dynamic power dissipation is particularly noticeable in the 2x4 decoder during switching events, when the 2-bit input activates one of the four output lines. A decoder's dynamic power performance is affected by the total power consumption, which is in turn affected by the switching rate and capacitance of the output lines.

Thirdly, there's static power dissipation, which happens even when transistors aren't switching because of leakage currents. With the growth of leakage currents and the shrinkage of transistor widths at advanced nodes like as 16 nm, this component has more importance.

4. Achieving Maximum Power Efficiency and Optimisation

Combining the minor transient spikes in power with the low average power

consumption of the decoder suggests that the design is well optimised for both static and dynamic power.To reach this level of power efficiency, the design most likely makes use of several strategies, including. Clock Gating: Disabling circuit components while they are not in use is typically done via clock gating in order to decrease wasteful switching activity.Dynamic power usage is significantly decreased with this strategy.

5. Operating at a Low Voltage:

Variability in the systemReduced impact:The consequences of manufacturing fluctuation at the 16 nm node may have been mitigated by the use of advanced design strategies like adaptive body biassing or transistor size, guaranteeing robust performance with minimum leakage currents. To further reduce subthreshold leakage current, the decoder might adopt Multi-Threshold CMOS (MTCMOS) approaches, which include using transistors with higher threshold voltages in non-critical pathways. This would further minimise leakage power.

6. How It Compares to Conventional Designs

The power findings indicate that the 2x4 decoder design in 16 nm technology outperforms the conventional designs used in earlier technology nodes (e.g., 45 nm or 28 nm) by a large margin. The decoder in 16nm technology has many advantages over these traditional devices, includingReduced Size Transistors:The result is an enhanced process, less power dissipation and capacitanceModern Technology:as a result, more efficient switching, greater control over leakage currents, and enhanced optimisation Methods: For example, clock gating, dynamic voltage scaling, and low-power logic approaches.

All of these things work together to make the decoder as efficient and effective as it is.

5. RESULT

The power research showed that the 2x4 decoder developed in 16nm technology had outstanding energy efficiency even under typical working settings, with an astonishingly low average power use of 5.617927e-07 watts.The highest power consumption occurred at 1.368324e-05, which corresponds to the transient switching events typical of digital circuitry, at 1.368324×10−5W1.368324.

This transient spike is supposed to be caused by activating the output lines in response to the 2-bit input.The lack of flow activity during the lean periods was suggested by the minimum power consumption of 1.440335 at 1 × 10−7, which is equivalent to a wave number of 1.440335.The design shows a balanced power profile with acceptable power spikes and low average dissipation, suggesting that the decoder is optimised for both performance and energy economy. These results demonstrate the decoder's usefulness for low-power, high-performance applications in modern digital systems, particularly at sophisticated technological nodes where power conservation is a major concern.

5. Conclusion

An examination of the 2x4 decoder's power consumption in 16 nm technology reveals an optimal design that strikes a good compromise between the two. Despite managing dynamic switching successfully, the decoder uses very little power on average. In addition to effectively managing transient power spikes and minimising leakage currents, the design guarantees energy-efficient operation, making it suitable for modern digital applications in low-power, high-performance devices in the sub-20nm technological century.

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