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Switched Inverter Comparator based 0.5 V Low Power 6-bit Flash ADC

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***Abstract*- This paper presents an ultra low power 6 bit Flash ADC designed in 180 nm CMOS technology for ultra low power applications. The design uses inverter based comparators to reduce the silicon area and power requirement. A novel clock delaying technique is used to power on the three stages of the comparator which work in series. This reduces the power consumption and increases speed of operation. Fat tree architecture is used to design the digital encoder. The power supply used for the design is 0.5 V and the sampling rate is 50 MS/s. The design consumes ultra low power of 600 μW and spans a very small area of 0.164 mm^2. In literature this is found to be the lowest for 6 bit ADCs in 180 nm with sampling frequency of 5 MS/s or above. The SNDR remains above 31.5 dB in the whole input frequency range of 0 to 25 MHz. The ADC has maximum DNL of 0.85 LSB and maximum INL of 1 LSB. The FOM of the ADC is found to be 0.39 pJ/conv.**

***Keywords*- Flash ADC, Inverter comparator, Low power, Low voltage, Fat tree encoder**

I. INTRODUCTION

The exponential growth in the usage of handheld, battery operated devices like cell phones, tablets, laptops and portable medical instruments has made power consumption one of the most prominent design criterion. Also as the fabrication cost of the chip is directly proportional to its area, there is a dire need for power efficient designs consuming a small area. Although process scaling and integration of all the necessary electronic circuits of diverse functions onto a single chip, called system on a chip (SoC), have reduced the total power consumption and required area of the devices and brought in great performance improvements, clever design choices can bring in further improvements in terms of power, speed and area.

Analog to digital converters are an essential part of any device which interacts with real world. The flash architecture of the ADC is the fastest one which is used as a building block for many architectures like folding and interpolating, pipelined, subranging ADCs etc. But the exponential increase in area and power consumption with resolution has limited the use of flash ADC in ultra low power applications.

The proposed ADC intends to fill the gap by proposing a 6 bit flash ADC for ultra low power applications which uses a small area. The present work builds upon our work presented in [1] and improves it in a number of ways with layout results. As power consumption reduces quadratically with the reduction of voltage [2], 0.5 V was chosen as the supply voltage. A novel technique of delayed clocks activating different stages of a modified inverter based comparator is used to reduce the power consumption and area when compared to OTA and Op Amp based comparators. Unlike threshold inverter quantizer (TIQ) which has a small fraction of the supply voltage as the input range, the proposed ADC has rail to rail input range. We have used low threshold MOSFETs in the design for the ultra low voltage operation of 0.5 V. The reference input for the ADC is generated from a resistor ladder network. The thermometer coded outputs of the comparators are converted into one-hot-code and the final digital output code is generated using a fat tree encoder.

In section 2 detailed explanation of the proposed comparator design is given. In section 3 the design of the 6 bit flash ADC using inverter comparator has been explained. The details of layout design and extracted layout simulation results are given in section 4 and section 5 concludes the paper.

II. DESIGN OF THE PROPOSED COMPARATOR

The use of inverter as a comparator was proposed in [3]. But because of its low gain and high parasitics inverter based comparator has not been exploited fully.

A scheme for voltage comparison using Inverter based comparator is shown in Fig. 1. In the figure, V_{IN} is the input signal, kV_{LSB} is the reference voltage of the k^{th} comparator and ΔV is the voltage difference between the two points on the characteristics (see Fig. 2) where gain of the inverter is equal to -1. The use of inverter as a comparator, shown in Fig.1, can be explained with respect to the two phases of the clock, φ and $\bar{\varphi}$. S_1, S_2 and S_3 are three switches and C_{INV} is the sampling capacitor.

Figure 2 shows the transfer characteristics of the inverter. In this figure, V_{mid} is the voltage when the output of the inverter is equal to the input.

During φ,
switches S_1 and S_3 are closed and S_2 is opened. The voltage across the capacitor V_C can be expressed in terms of V_{IN} and V_{mid} of the inverter as,

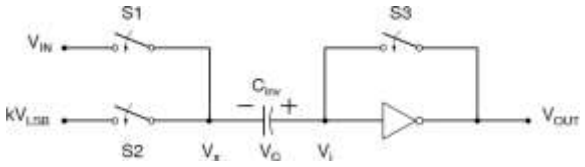


Fig. 1. Inverter comparator

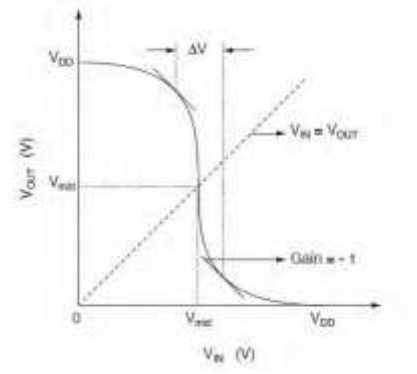


Fig. 2. CMOS inverter characteristics

$$\begin{aligned} V_I &= V_{mid} \\ V_C &= V_I - V_X \\ &= V_{mid} - V_{IN} \end{aligned} \tag{1}$$

During $\bar{\varphi}$,

switches S_1 and S_3 are opened, S_2 is closed connecting kV_{LSB} to V_X. Now, the input of the inverter V_I is calculated with the help of (1) as,

$$\begin{aligned} V_I &= V_C + kV_{LSB} \\ &= (V_{mid} - V_{IN}) + kV_{LSB} \\ &= V_{mid} - (V_{IN} - kV_{LSB}) \end{aligned} \tag{2}$$

Now, depending on the value of $(V_{IN} - kV_{LSB})$, the output of the inverter will be decided as follows,

$$\begin{aligned} (V_{IN} - kV_{LSB}) > \frac{\Delta V}{2} &\Rightarrow V_I < V_{mid} - \frac{\Delta V}{2} \\ V_I < V_{mid} - \frac{\Delta V}{2} &\Rightarrow V_{OUT} = \text{'1'} \\ (V_{IN} - kV_{LSB}) < -\frac{\Delta V}{2} &\Rightarrow V_I > V_{mid} + \frac{\Delta V}{2} \\ V_I > V_{mid} + \frac{\Delta V}{2} &\Rightarrow V_{OUT} = \text{'0'} \end{aligned} \tag{3}$$

The low gain of the inverter and the parasitics associated with the sampling capacitor, switches and the switching kickback noise hinder the performance of the inverter comparator thereby making it unsuitable for low voltage and high speed operation. These limitations are overcome by adding a second inverter stage which is designed to increase the gain and clocked cleverly to nullify the effect of kickback noise and parasitics. A third stage of back to back inverters is added to further increase the gain and to hold the comparator output for digitization. The proposed comparator design is shown in Fig. 3. Figure 4 shows the clock signals used in Fig. 3.

Stage 1 of the comparator works as explained above. When $\bar{\varphi}$ goes high, the reference voltages are connected to the comparators. Hence there is a sudden current flow from the resistor ladder network to all the comparators of the ADC to charge the respective capacitors C_{inv}. This disturbs the reference voltages. The altered reference voltages would change the actual $(V_{IN} - kV_{LSB})$ values temporarily which may start driving the inverter Inv1 towards wrong output. Actual $(V_{IN} - kV_{LSB})$ values will be slowly restored once the C_{inv} capacitors are charged. But the output of the Inv1 will take much longer time to reflect the correct output, making the entire operation very slow. To overcome this, Stage 2 is clocked after a while, allowing reference voltages and kickback noises to settle. When φ_{d1} is applied, it connects the output of *Inv2* to its input driving V_{O1} and V_{O2} to V_{mid}. This brings back the disturbed output of *Inv1* to V_{mid}. When φ_{d1} goes low, *Inv1* gives the correct output according to the settled values of $(V_{IN} - kV_{LSB})$. This output is further enhanced by *Inv2*. Now φ_{d2} is applied to the back to back connected inverters shorting their output to input making them equal to V_{mid}. When φ_{d3} is applied, the back to back inverters drive the *Inv2* output to either supply voltage or ground resulting in high speed operation. They also act as a latch and hold the value till φ_{d2} goes high in the next cycle. This eliminates the need for a separate latch to hold the comparator outputs for the digital encoding.

III. ADC DESIGN

The block diagram of the ADC is shown in Fig. 5. The individual blocks are explained in the following subsections.

A. Reference Generation

The reference voltage for the comparators is generated by a resistor ladder network. The resistor ladder has been split into two parts: one generating the reference voltages for the odd numbered comparators (k = 1, 3, 5 etc.) and the other for even numbered comparators (k = 2, 4, 6 etc.). This reduces the RC delay of the resistor ladder and makes laying out the ADC easier. The individual resistor values are selected for optimum speed and power consumption.

B. Clock Generation

As explained in section II, the different stages of the

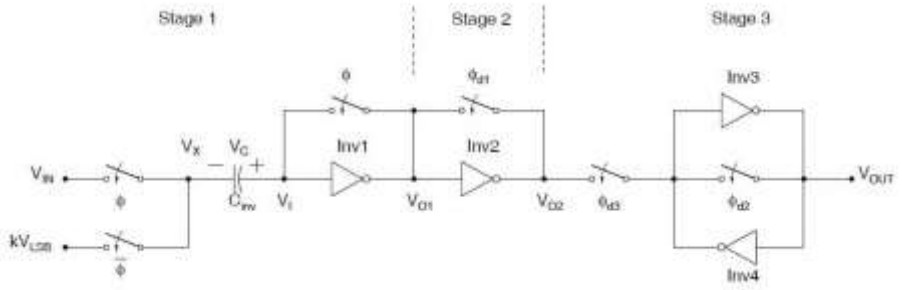


Fig. 3. Proposed Inverter Comparator

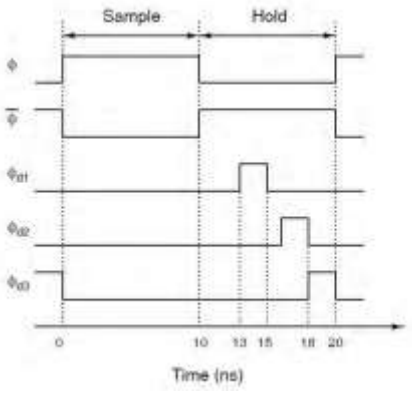


Fig. 4. Clock signals for the proposed design

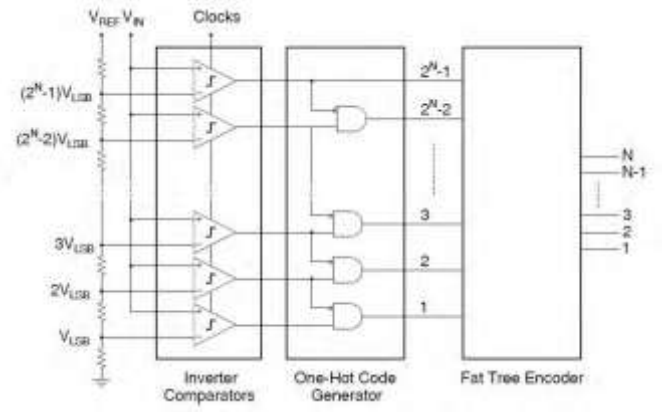


Fig. 5. Block diagram of the ADC

comparators are clocked cleverly to nullify the effect of reference variation and kickback noises achieving high speed operation. φ is generated from the system clock using buffers. $\overline{\varphi}$ is generated by inverting φ. φ_{d1} is generated by delaying φ and ANDing the delayed version with $\overline{\varphi}$. φ_{d2} and φ_{d3} are the delayed versions of φ_{d1}. Inverter buffers are used as delay elements in the design as they occupy small area and consume very low power.

C. Encoder

The output of the comparators will be thermometer coded. For converting the thermometer code to 6 bit binary code fat tree architecture is used. Fat tree architecture is one of the fastest architectures and it uses relatively small area when compared to commonly used ROM encoder [4]. The drawback is that, laying out a fat tree encoder is challenging as it has a tree structure and not as regular as a ROM encoder. For feeding the inputs of the fat tree encoder, thermometer code will have to be converted into one-hot-code. This can be easily achieved by using a NOT and AND gate combination as shown in Fig. 5. The one-hot-code is given as the input to the fat tree encoder. The fat tree encoder converts the one-hot-code into binary code using multiple tree structures.

IV. Layout Details And Simulation Results

The whole design has been laid out in UMC 180 nm CMOS technology. For the ultra low voltage operation of 0.5 V, low V_{th} transistors have been used in the design. Careful sizing of the inverters in the comparators, using low V_{th} PMOS as sampling capacitor C_{inv} and the optimum sizing of the switches along with the split resistor network have improved the overall ADC performance over [1]. Figure 6 shows a single inverter comparator layout along with its dimensions. Figure 7 shows the complete layout of the ADC.

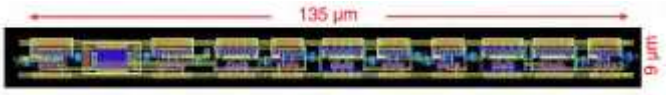


Fig. 6. Layout of a single inverter comparator

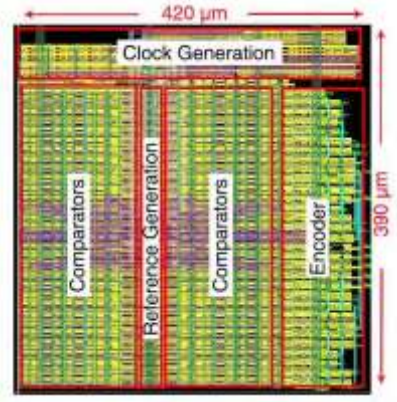


Fig. 7. Layout of the ADC

The total area consumed by the ADC is 0.164 mm^2. The measured differential non linearity (DNL) and integral non linearity (INL) of the ADC are shown in Fig. 9. The maximum DNL and INL are found to be 0.85 LSB and 1 LSB respectively. There are no missing codes in the output. The dependency of the spurious free dynamic range (SFDR) and signal to noise and distortion ratio (SNDR) on input frequency is shown in Fig. 9 for the sampling frequency of 50 MS/s. Figure 10 shows the power spectrum of the reconstructed output of the ADC for the input frequency of 23.83 MHz. At zero frequency, the DC component superimposed on the input can be seen. Power spectrum has been calculated by performing 128 point FFT of the output. A 96% full scale input (480 mV peak to peak) has been used for all calculations. At the input frequency of 23.83 MHz, SNDR is found to be 31.5 dB giving effective number of bits (ENOB) as 4.97. The SNDR remains above this value for all the lower input frequencies. The performance of the ADC against temperature is shown in Fig. 11 and Fig. 12. The power consumption increases with temperature due to increase in leakage currents but the SNDR is not affected. The SNDR variation against process variation is shown in Fig. 13. All these simulations have been carried out at Nyquist frequency as that depicts the worst case scenario. The ADC consumes an ultra low power of 600 µW at room temperature.

The popular figure of merit (FOM) used to compare the ADCs is calculated as [5],

$$FoM = \frac{Power}{2 \cdot f_{in} \cdot 2^{ENOB}} \quad \text{(fJ/conv)} \qquad (4)$$

The FOM of the ADC is 0.39 pJ/conv. Table I summarizes the overall performance of the ADC.

Table II compares the performance of the present work with recently published state of the art designs. The work presented in this paper is better than almost all the 180 nm designs in terms of power consumption, speed and area requirement. It is also better than many of the 130 nm and some of the 90 nm and 65 nm designs which have the advantage of lower power consumption, lower parasitics and smaller area.

TABLE I

PERFORMANCE SUMMARY OF THE ADC

Parameter	Value
Technology	UMC 180 nm CMOS, Low V_{th} transistors
Supply Voltage	0.5 V
Resolution	6 bit
Sampling Frequency	50 MS/s
Input Range	490 mV peak to peak
SFDR at 23.83 MHz	36.9 dB
SNDR at 23.83 MHz	31.5 dB
ENOB at 23.83 MHz	4.97 bits
Maximum DNL, INL	0.85 LSB, 1 LSB
Total Power	600 µW
FOM	0.39 pJ/conv
Total Area	0.164 mm^2

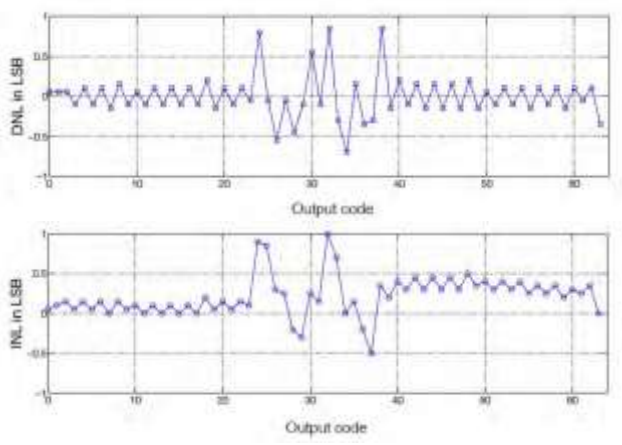


Fig. 8. DNL and INL plot of the ADC

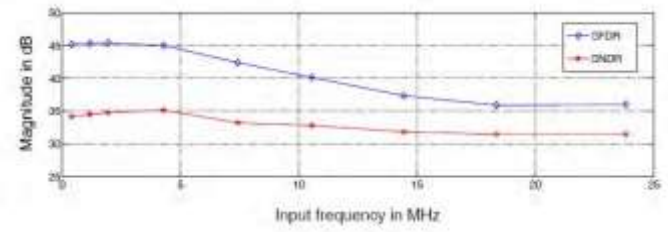


Fig. 9. SFDR and SNDR variation of the ADC with input frequency

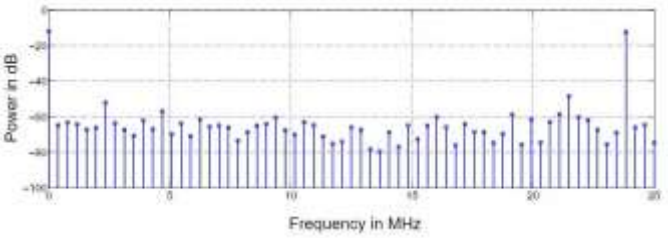


Fig. 10. ADC power spectrum with input frequency of 23.83 MHz

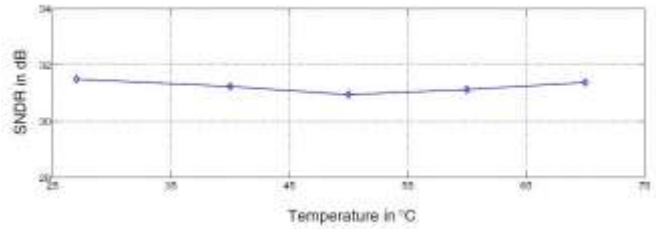


Fig. 11. SNDR variation of the ADC with temperature

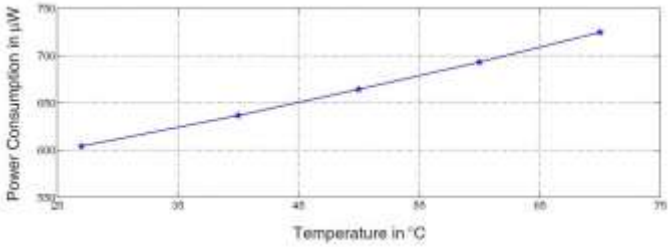


Fig. 12. Power consumption of the ADC with temperature

TABLE II
COMPARISON WITH LOW VOLTAGE STATE OF THE ART DESIGNS

Reference	Type	V_{DD} (V)	Resolution (bits)	Speed (MS/s)	Power (mW)	ENOB	Area (mm^2)	Technology (nm)	FOM (pJ/conv)
[6] - Apr/2009	Flash	1.2	6	100	4	5.63	0.13	65	0.8
[7] - 2010	Flash	0.35	4	200	0.54	3.03	0.0075	90	0.33
[8] - Nov/2008	Inverter Flash	0.6	5	60	1.3	4.36	0.11	90	1.06
[9] - Feb/2011	Pipeline	1.2	10	40	15.6	9.01	1.76	130	0.22
[10] - Aug/2011	Pipeline	1.2	10	60	23	9.16	1.84	130	0.67
[11] - Jan/2011	Flash	1.8	4	700	5.56	3.77		180	0.46
[12] - Nov/2009	Flash	0.4	6	0.4	0.0017	5.05	1.96	180	0.125
[13] - Feb/2009	Folding	1.2	8	80	30	6.94	1	180	3.1
[14] - July/2008	Pipeline	1.8	8	200	22	7.24	0.32	180	0.74
[15] - Mar/2010	Pipeline	1.8	10	60	18	8.6	0.84	180	1.15
[16] - May/2010	Pipeline	1.8	10	100	31	8.5	1.28	180	0.85
[17] - Jan/2010	Pipeline	1.8	11	40	21	10.5	2.1	180	0.18
Proposed Work	Inverter Flash	0.5	6	50	0.6	4.97	0.164	180	0.39

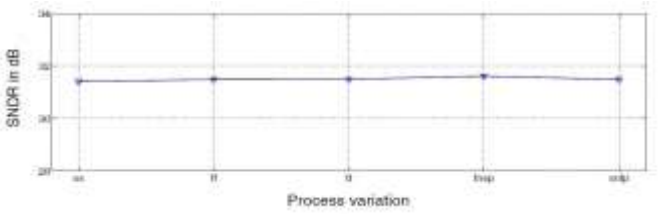


Fig. 13. SNDR variation of the ADC with process variation

V. CONCLUSION

As it can be seen from the literature, there have not been many low voltage ultra low power ADC designs in 180 nm technology. The present work has a relatively better FOM consuming ultra low power and very small area while achieving respectable speed of 50 MS/s. The ADC can be used in battery operated devices where power efficiency is very important criterion. It can also be used as a building block in the design of high resolution pipelined, folding-interpolating and subranging ADCs. The porting of the design to a lower technology node can bring in further improvement in the performance of the ADC.

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